REMARKS

The present application was filed on April 6, 2007 with claims 1-31. Claims 1-31 remain pending. Claims 1, 11, 21, 24, and 27 are the pending independent claims.

In the present Office Action, claims 1-5, 11-15, 21 and 23-30 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Publication No. 2005/0146923 A1 to Lee et al. (hereinafter "Lee").

Claims 6 and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Publication No. 2005/0146932 A1 (Lee) in view of U.S. Patent No. 6920067 to Hsu et al. (hereinafter "Hsu").

Claims 7-10, 17-20, 22 and 31 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Publication No. 2005/0146932 A1 (Lee) in view of U.S. Patent No. 5751635 to Wong et al. (hereinafter "Wong").

In this response, Applicant respectfully traverse the rejections and amended independent claims 1, 11, 21 and 27 and dependent claim 25. Applicants respectfully request reconsideration of the present application in view of the remarks to follow.

With regard to the §102(e) rejection, Applicants initially note that MPEP §2131 specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). For the reasons identified below, Applicants submit that the Examiner has failed to establish anticipation of claims 1-5, 11-15, 21 and 23-30 by Lee.

In formulating the §102(e) rejection of independent claim 1, the Examiner recites that Lee "proposes a method for programming a one time programmable memory" citing Lee page 4 paragraph [0052]. Applicant respectfully disagrees and argues that the memory cell that Lee teaches in paragraphs [0001]-[0051] and in FIGs. 1-11 is not a one time programmable memory cell and therefore the programming method that Lee teaches in paragraphs [0001]-[0051] is not for the programming of the one-time programmable (OTP) cell in paragraph [0052]. To establish

that the memory cell Lee teaches in paragraphs [0001]-[0051] and FIGs 1-11 is not a one time programmable cell, consider that Lee teaches it is erasable and therefore reprogrammable. Lee, page 4 paragraph [0052], defines an OTP cell as "can be programmed one time only." As is known in the art, a cell that can be erased can then be reprogrammed. On page 1, paragraph [0005], Lee states "A single-poly EPROM (erasable programmable read only memory) cell is then proposed to prevent process incompatibility issue." On page 2, paragraph 30, Lee states "In general, the invention at least introduces, for example a single poly electrically programmable EPROM cell ... to prevent over-erase issues." On page 2, paragraph [0031], Lee states "a novel design of a compact single-poly EPROM/EEPROM memory cell that is named Shared Couple Capacitor Single Poly EPROM/EEPROM (SCCSP Cell as shown in FIG 2) is proposed." Applicant suggests, as is known in the art, that EEPROM is an acronym for electrically erasable programmable read only memory. Lee in FIGs. 6, 7 and 8 describes both cell programming and cell erasure.

Applicant respectfully argues that, as known in the art, an erasable and programmable cell, as are EPROM and EEPROM cells, is not one time programmable but multi time programmable. Furthermore, Lee on page 4, in paragraph [0052], does not teach the one time programmable cell operation or programming. In paragraph [0053], Lee proposes use of his aforementioned SCCSP cell as the OTP cell mentioned in paragraph [0052]. However, as taught in Lee's specification and Figures, the SCCSP cell is configured to be erased as well as programmed and therefore is not a one time programmable cell. With consideration of the above, Applicant respectfully submits that the OTP cell of Lee in paragraph [0052] is not taught by Lee to follow the programming method comprising programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.

Applicants respectfully disagree with Examiner's rejections of independent claims 11, 21 and 27, and dependent claim 25 at least for the same reasons as Applicants present for claim 1.

In formulating the §102(b) rejection of claim 24, the Examiner recites that Lee proposes a memory cell comprising only one transistor. The Examiner references Lee FIG 1 and page 1 paragraph [0006]. Applicants respectfully disagree. Lee's FIG 1 shows a memory cell clearly comprising two transistors, an NMOS transistor formed within a P-type substrate (left side of

FIG. 1) and a PMOS transistor formed within an N-well (right side of FIG. 1). Lee paragraph [0006] recites "In FIG. 1A, an NMOS transistor with the gate FG is forming on a p-type substrate. However, in order to have the capability to store the binary data, the PMOS transistor is formed in N-well to serve the capacitor function." Clearly, the memory cell of FIG.1 and described in paragraph [0006] is a two transistor memory cell comprising two coupled transistors. Independent claim 24 is patentable because it is not anticipated by Lee.

Dependent claims 25 and 26 are patentable at least by virtue of their dependency upon independent claim 24.

In formulating the §102(b) rejection of claim 27, the Examiner recites that Lee "discloses an integrated circuit." Examiner references page 1 paragraph [0001] which recites only "1. Field of Invention." Applicants respectfully disagree. Nowhere does Lee propose that his invention is or is related to an integrated circuit. The terms "integrated circuit" or "IC" are not used within Lee. Independent claim 27 is patentable because it is not anticipated by Lee.

In formulating the §103(a) rejection of claim 10, the Examiner recites that Lee discloses "evaluating a rate of voltage decay of at least one column in said array of transistors." Examiner references Lee FIG. 4 and page 3 paragraph [0043]. Applicants respectfully disagree. Lee FIG. 4 and paragraph [43] present the voltages applied for read operations. They do not address nor mention evaluating a rate of voltage decay or any equivalent.

Notwithstanding the traversal, Applicant has amended independent claims 1, 11, 21 and 27, and dependent claim 25. Applicant's claims 1, 11, 21, 25 and 27, as amended, now recite: wherein the hot carrier aging comprises injection of carriers into a gate oxide, and wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps.

Support for the amendments to claims 1, 11, 21 and 27 can be found in the specification at, for example, page 2 paragraph [0018], FIG. 5A and FIG. 6A (referring to U.S. Patent Application Publication No. 2007/0274126 A1)

Dependent claims 2-10, 12-20, 22-23 and 28-31 are patentable at least by virtue of their dependency upon independent claims 1, 11, 21 and 27. Dependent claim 10 is also patentable at least because it is not anticipated by Lee.

Given the foregoing traversal, Applicant submits that the amendments made herein are not made for reasons relating to patentability over Lee, in that the teachings of the Lee reference

fails to meet the limitations of the claims as previously presented. Instead, the amendments are made solely in order to expedite the prosecution of the application

In light of the above remarks and amendments, Applicants respectfully submit that claims 1-31 are in condition for allowance and request the withdrawal of the §102(e) and §103(a) rejections.

Respectfully submitted,

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